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09/635,124	08/08/2000	Norio Fukasawa	980233A	4720

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ARMSTRONG,WESTERMAN & HATTORI, LLP
1725 K STREET, NW.
SUITE 1000
WASHINGTON, DC 20006

EXAMINER
GRAYBILL, DAVID E

ART UNIT	PAPER NUMBER
2827	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/635,124	FUKASAWA ET AL.
	Examiner	Art Unit
	David E Graybill	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5,7-10,12,21,22,24-29,32-35,37-40,45-53,65-69,78,86 and 88-90* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *see 6)* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *IDS papers No. 11-13 and 16* .

Continuation of Disposition of Claims: Claims pending in the application are 1,4,5,7-10,12,21,22,24-29,32-35,37-40,45-53,65-69,78,86 and 88-90.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submissions filed on 2-6-2 and 7-1-2 have been entered.

Claims 12, 27, 28, 32/30, 40, 45-53 and 33/32/30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 12, 32/30, 40, 45-53 and 33/32/30 are rejected as incomplete because they depend on canceled claims. See MPEP 608.01(n)V.

The following lack sufficient antecedent basis:

Claim 27, "the cutting position grooves filled with the sealing resin";

Claim 28, "the position interposed between the pair of stress relaxing grooves";

Claim 68, "the heat radiating member";

Claim 88, "the second mold half body."

In claim 33 the scope of the limitation, "the positioning grooves can be formed by subjecting the back surface to half scribing" cannot be determined because the conditions or circumstances which enable the practice of the potential process limitation, "can be formed by subjecting the back surface to half scribing" are not recited, and cannot otherwise be determined.

Claims 27, 28 and 68 have not been rejected over the prior art because, in light of the 35 U.S.C. 112 rejections supra, there is a great deal of confusion and uncertainty as to the proper interpretation of the limitations of the claims; hence, it would not be proper to reject the claims on the basis of prior art. As stated in In re Steele, 305 F.2d 859, 134 USPQ 292 (CCPA 1962), a rejection should not be based on considerable speculation about the meaning of terms employed in a claim or assumptions that must be made as to the scope of the claims. See also MPEP 2173.06.

In the rejections infra, reference labels are generally recited only for the first recitation of identical claim language.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1 and 35 are rejected under 35 U.S.C. 102(e) as being anticipated by Lim (5925934).

At column 6, line 61 to column 9, line 8, and column 10, lines 4-14, Lim teaches the following:

1. A method for fabricating a semiconductor device comprising: a resin sealing step of loading a substrate 570 on which

semiconductor elements having protruding electrodes 520 are formed to a mold 615, and supplying a sealing resin 545 to positions of the protruding electrodes so as to form a resin layer which seals the protruding electrodes and the substrate; a protruding electrode exposing step of exposing at least ends of the protruding electrodes from the resin layer; and a separating step of cutting the substrate together with the resin layer so that the semiconductor elements are separated from each other, wherein the resin sealing step disposes a film 570 between the protruding electrodes and the mold [top mold half] which thus contacts the sealing resin through the film.

35. The method for fabricating the semiconductor device as in 1, wherein the sealing resin is processed in positions in which positioning protruding electrodes 520 are formed in order to discriminate the protruding electrodes and the positioning protruding electrodes from each other.

To further clarify the teaching of a separating step of cutting the substrate together with the resin layer, as cited, Lim teaches "excising" the substrate, portions of which remain encapsulated together with the resin layer.

To further clarify the teaching wherein the sealing resin is processed in positions in which positioning protruding electrodes are formed in order to discriminate the protruding

electrodes and the positioning protruding electrodes from each other, it is noted that the resin is processed in order to distinguish each of the electrodes from each other by exposing differences in locations of the electrodes.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 4 and 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lim as applied to claims 1 and 35, and further in combination with Ohta (5641997).

Lim does not appear to explicitly teach the following: 4. The method for fabricating the semiconductor device as in 1 wherein: the mold used in the resin sealing step comprises an upper mold which can be elevated, and a lower mold having a first lower mold half body which is kept stationary and a second lower mold half body which can be elevated with respect to the first lower mold half body; and the resin sealing step comprises: a substrate loading step of placing the substrate on which the semiconductor elements having the protruding electrodes are arranged in a cavity defined by a cooperation of the first and second lower mold half bodies and providing the sealing resin the cavity; a resin layer forming step of moving down the upper mold and the second lower mold half body so that the sealing resin is heated, melted and compressed so that the resin layer sealing the protruding electrodes is formed; and a detaching step of moving up the first mold so as to detach the upper mold from the resin layer, and then moving down the second lower mold half body from the first lower mold half body so that the substrate to which the resin layer is provided is detached from the mold.

88. A method for fabricating the semiconductor as in 4, wherein the resin sealing step further comprises a film disposing step of providing a non-adhesive process film between contact surfaces of the upper mold and the first lower mold half body and the second mold half body.

Nonetheless, at column 6, lines 32-65, column 7, lines 13-19, column 9, lines 23-34, column 11, lines 15-63, and column 54, lines 56-64, Ohta teaches wherein a mold used in a resin sealing step comprises an upper mold 9a which can be elevated, and a lower mold having a first lower mold half body 8b which is kept stationary [after clamping] and a second lower mold half body 9b which can be elevated with respect to the first lower mold half body; and a resin sealing step comprises: a substrate loading step of placing a substrate 3 on which a semiconductor element 5 having protruding electrodes 4 is arranged in a cavity defined by a cooperation of the first and second lower mold half bodies and providing the sealing resin 1 in the cavity; a resin layer forming step of moving down the upper mold and moving the second lower mold half body so that the sealing resin is heated, melted and compressed so that the resin layer sealing the protruding electrodes is formed, a detaching step of moving the mold so as to detach the upper mold from the resin layer, and so that the substrate to which the resin layer is provided is

detached from the mold, wherein the resin sealing step further comprises a film disposing step of providing a non-adhesive process film ["releasing agent"] between contact surfaces of the upper mold and the first lower mold half body and the second mold half body. Additionally, it would have been obvious to combine the process of Ohta with the process of Lim because it would facilitate resin sealing.

Although the applied prior art does not appear to explicitly teach the entire particular mold moving sequence, as cited, Ohta teaches that the upper mold half and the second lower mold half body are movable up and down, and it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed mold moving sequence because applicant has not disclosed that the sequence is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical. Moreover, it is well established that, in a well known process, the order of performing process steps is prima facie obvious in the absence of new or unexpected results. Ex parte Rubin 128 USPQ (PO BdPatApp 1959).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lim as applied to claims 1 and 35, and further in combination with Ohta (5641997).

Lim does not appear to explicitly teach the following: 5. The method for fabricating the semiconductor device as in 1, wherein: an excess resin removing mechanism is provided in the mold used in the resin sealing step; and the excess resin removing mechanism removes excess resin and controls a pressure applied to the sealing resin in the mold. Notwithstanding, as cited supra, Ohta teaches this process. Moreover, it would have been obvious to combine the process of Ohta with the process of Lim because it would facilitate resin sealing.

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lim as applied to claims 1 and 35, and further in combination with Ota (JP5343458).

Lim does not appear to explicitly teach the following: 7. The method for fabricating the semiconductor device as in 1, wherein the sealing resin is provided to the film before the resin sealing step is executed.

8. The method for fabricating the semiconductor device as in 7, wherein a plurality of sealing resins are provided to the film, and the resin sealing step is continuously carried out by moving of the film.

Nevertheless, in the English abstracts and figures, Ota teaches wherein a sealing resin 2 is provided to a film 7 before a resin sealing step is executed, a plurality of sealing resins 1, 2 are provided to the film, and the resin sealing step is continuously carried out by moving of the film. In addition, it would have been obvious to combine the process of Ota with the process of Lim because it would facilitate resin sealing.

Claims 1, 24, 25 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Kihira (JP864725) and Tanaka (JP63308329).

In the English abstract, translation and figures, Kihira teaches the following:

1. A method for fabricating a semiconductor device comprising: a resin sealing step of loading a substrate 11 on which semiconductor elements having protruding electrodes 16 are formed to a mold 21a, 21b, and supplying a sealing resin 19 to positions of the protruding electrodes so as to form a resin layer which seals the protruding electrodes and the substrate; a protruding electrode exposing step of exposing at least ends of the protruding electrodes from the resin layer; and a separating step of cutting the substrate together with the resin layer so that the semiconductor elements are separated from each other.

However, Kihira does not appear to explicitly teach wherein the resin sealing step disposes a film between the protruding electrodes and the mold which thus contacts the sealing resin through the film, and the following:

24. The method for fabricating the semiconductor device as in 1, wherein: the film used in the resin sealing step has projections located in positions corresponding to those of the protruding electrodes; and the resin layer is formed in a state in which the projections are pressed against the protruding electrodes.

34. The method for fabricating the semiconductor device as in 1, wherein: the film used in the resin sealing step has projection or recess portions located in positions in which the film is not interfered with the projecting electrodes; and recess or projection portions formed on the resin layer by the projection or recess portions are used for positioning after the resin sealing step is completed.

Nonetheless, in the English abstracts and figures, Tanaka teaches wherein a resin sealing step disposes a film 17 between protruding electrodes 12 and a mold 14, 15 which thus contacts the sealing resin 18 through the film, the film used in the resin sealing step has projections located in positions corresponding to those of the protruding electrodes, the resin layer is formed in a state in which the projections are pressed

against the protruding electrodes, the film used in the resin sealing step has projection portions located in positions in which the film is not interfered with the projecting electrodes, and recess portions formed on the resin layer by the projection portions are used for positioning after the resin sealing step is completed.

To further clarify the teaching that the recess portions formed on the resin layer by the projection portions are used for positioning after the resin sealing step is completed, it is noted that the purpose of the recess portions of Tanaka is to expose the electrodes for electrical connection, and it is inherent in the process of electrode connection that they are used for positioning.

In addition, in the combination of Kihira and Tanaka, Kihira teaches the following:

25. The method for fabricating the semiconductor device as in 1, wherein: an external connection protruding electrode forming step is executed which forms external connection protruding electrodes 20 on the ends of the protruding electrodes after the ends of the protruding electrodes are exposed from the resin layer in the protruding electrode exposing step.

Claims 9, 10, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Kihira and Tanaka

as applied to claims 1, 24, 25 and 34, and further in combination with Lerner (5381042).

Kihira and Tanaka do not appear to explicitly teach the following:

9. The method for fabricating the semiconductor device as in 1, wherein, a reinforcement plate is loaded onto the mold before the substrate is loaded onto the mold in the resin sealing step.

10. The method for fabricating the semiconductor device as in 9, wherein the reinforcement plate comprises a substance having a heat radiating performance.

21. The method for fabricating the semiconductor device as in 9, further comprising a reinforcement plate to which the sealing resin is provided beforehand in the resin sealing step.

22. The method for fabricating the semiconductor device as in 21, wherein: a frame extending towards the substrate in a state in which the reinforcement plate is loaded onto the mold is formed to define a recess portion; and the resin layer is formed on the substrate by using, as a cavity for resin sealing, the recess portion in the resin sealing step.

Nonetheless, at column 4, line 29 to column 5, line 64, Lerner teaches wherein, a reinforcement plate 400 is loaded onto a mold 500 before a substrate 521 is loaded onto the mold in a resin sealing step, the reinforcement plate comprises a

substance having a heat radiating performance, a reinforcement plate to which the sealing resin 601 is provided beforehand [before the package 600 is removed] in the resin sealing step, and a frame 400 extending towards the substrate in a state in which the reinforcement plate is loaded onto the mold is formed to define a recess portion 510, and the resin layer is formed on the substrate by using, as a cavity for resin sealing, the recess portion in the resin sealing step. In addition, it would have been obvious to combine the process of Lerner with the process of Kihira and Tanaka because it would improve heat dissipation.

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Kihira and Tanaka as applied to claims 1, 24, 25 and 34, and further in combination with Lynch (5698465).

Kihira and Tanaka does not appear to explicitly teach the following:

26. The method for fabricating the semiconductor device as in 25, wherein the protruding electrodes and the external connection protruding electrodes are bonded by using a bonding member having a characteristic of stress relaxation in the external connection protruding electrode forming step.

Notwithstanding, at column 4, lines 60-65, Lynch teaches wherein a protruding electrode 26 and an external connection protruding electrode 36 are bonded by using a bonding member 36 having a characteristic of stress relaxation in an external connection protruding electrode forming step. Moreover, it would have been obvious to combine the process of Lynch with the process of the applied prior art because it would provide an external connection protruding electrode.

Claim 29 is rejected under 35 U.S.C. 102(b) as being anticipated by Badehi (5455455).

At column 6, line 39 to column 7, line 30, and column 12, lines 46-60, Badehi teaches the following:
29. A method for fabricating semiconductor devices comprising: a first separating step of cutting a substrate 20 on which semiconductor elements 40 having protruding electrodes 34 are formed so that the semiconductor elements are separated from each other; a resin sealing step of arranging the separated semiconductor elements on a base member 42 and sealing a sealing resin 44 so that a resin layer is formed; a protruding electrode exposing step of exposing at least ends of the protruding electrodes from the resin layer; and a second separating step of cutting the resin layer together with the base member in positions 50 between adjacent semiconductor elements, so that

the semiconductor elements to which the resin layer is formed are separated from each other.

Claims 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lim as applied to claims 1 and 35, and further in combination with Romano (4887149).

Lim does not appear to explicitly teach the following: 32. The method for fabricating the semiconductor device as in 1, wherein positioning grooves are formed on a back surface of the resin layer of the substrate after the resin sealing step is executed and before the separating step is executed.

Nevertheless, at column 3, line 65 to column 5, line 54, Romano teaches wherein positioning grooves 7, 7', 8, 8' are formed on a back surface of a resin layer 5, 6 of a substrate 13 after a resin sealing step is executed. In addition, it would have been obvious to combine the process of Romano with the process of Lim because it would facilitate positioning of the semiconductor device on a heat sink.

Although the applied prior art does not appear to explicitly teach that the positioning grooves are formed before the separating step is executed, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed sequence because

applicant has not disclosed that the sequence is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical. Moreover, it is well established that, in a well known process, the order of performing process steps is prima facie obvious in the absence of new or unexpected results. Ex parte Rubin 128 USPQ (PO BdPatApp 1959).

The applied prior art also does not appear to explicitly teach the following:

33. The method for fabricating the semiconductor device as in 32 characterized in that the positioning grooves can be formed by subjecting the back surface to half scribing.

Nonetheless, this limitation is merely a potential process which does not result in a manipulative difference as compared to the process of the applied prior art. Furthermore, because the process of the applied prior art is inherently capable of practicing the potential process, the potential process limitation does not patentably distinguish the claimed process from the process of the applied prior art.

Claims 37-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Yasunaga (JP6302604).

In the English abstract, translation and figures, Yasunaga teaches the following:

37. A method for mounting a semiconductor device, comprising mounting the semiconductor device on a mounting board so as to vertically stand thereon the semiconductor device comprising: a semiconductor element 3 having a surface on which external connection electrodes 4 are provided which are to be electrically connected to external terminals 10, and a resin layer 1 provided on the surface of the semiconductor element so as to cover the external connection electrodes, wherein the external connection electrodes are exposed at a lateral surface of the resin layer.

38. The method for mounting the semiconductor device as in 37, wherein a plurality of semiconductor elements 3a, 3b are arranged side by side so that adjacent ones of the semiconductor elements are bonded by an adhesive 1.

39. The method for mounting the semiconductor device as in 37 wherein a plurality of semiconductor elements are arranged side by side so as to vertically stand by supporting members 70.

Claim 89 is rejected under 35 U.S.C. 102(a) as being anticipated by Kihira (JP864725).

As cited supra, Kihira teaches the following:

89. A method for fabricating a semiconductor device, comprising the steps of: an encapsulating step of supplying a rigid sealing material 19 to a substrate on which protruding electrodes are

formed so as to form an encapsulation layer which seals the protruding electrodes and the substrate; a stiffening step of heating the encapsulation layer; a protruding electrode exposing step of exposing at least ends of the protruding electrodes from the resin layer; and a separating step of cutting the substrate together with the resin layer so that the semiconductor elements are separated from each other.

Claims 65-67 and 69 are rejected under 35 U.S.C. 102(b) as being anticipated by Herndon (4027383).

At column 3, line 60 to column 6, line 9, Herndon teaches the following:

65. A method for fabricating a semiconductor device comprising: an electrode plate forming step of forming a pattern on a metallic base so that an electrode plate 26A is formed; a chip mounting step of mounting semiconductor elements 54 on the electrode plate and electrically connecting the semiconductor elements thereto; a sealing resin 74 forming step of forming a sealing resin which seals the semiconductor elements and the electrode plate; and a cutting step of cutting the sealing resin and the electrode plate at boundaries between adjacent ones of the semiconductor elements so that the semiconductor devices are separated from each other.

66. The method for fabricating the semiconductor device as, in 65, wherein the pattern is formed in the electrode plate forming step by etching or press processing.

67. The method for fabricating the semiconductor device as in 65 wherein the semiconductor elements are mounted, in the chip mounting step, on the electrode plate in a flip-chip bonding formation.

69. The method for fabricating the semiconductor device as in 65, wherein: protruding terminals 76 protruding from the electrode plate are formed in the electrode plate forming step; and the sealing resin is formed, in the sealing resin forming step, so as to expose the protruding terminals from the sealing resin.

Claim 86 is rejected under 35 U.S.C. 102(b) as being anticipated by Yamaji (5394303).

At column 2, line 51 to column 4, line 34, Yamaji teaches the following:

86. A method for fabricating a semiconductor device, comprising: a semiconductor device main body forming step of forming a semiconductor device main body 1 having a semiconductor element having a surface on which protruding electrodes 2_1, 2_2 are directly formed, and a layer 4 which is formed on the surface of the semiconductor element and seals the protruding electrodes

except for ends thereof; an interposer forming step of forming an interposer 3 to which the semiconductor device main body is attached, a wiring pattern 7_1 to which the semiconductor device main body is connected being formed on a base member of the interposer; a conductive member arranging step of arranging a conductive member 5_1 to at least one of the semiconductor device main body and the interposer; a bonding step of bonding the semiconductor device main body and the interposer by an adhesive 4 and connecting them electrically; and an external connection terminal forming step of forming external connection terminals 6_3, 6_4 which are connected to the wiring pattern through holes 8 formed in the base member and are arranged on a surface of the semiconductor device main body opposite to the surface on which the protruding electrodes are provided.

Claim 78 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji as applied to claim 86, and further in combination with Pennisi (5136365)

As cited supra, Yamaji teaches the following:

78. A method for fabricating a semiconductor device, comprising: a semiconductor device main body forming step of forming a semiconductor device main body having a semiconductor element having a surface on which protruding electrodes are directly formed, and a layer which is formed on the surface of the

semiconductor element and seals the protruding electrodes except for ends thereof; an interposer forming step of forming an interposer to which the semiconductor device main body is attached, a wiring pattern to which the semiconductor device main body is connected being formed on a base member of the interposer; a bonding step of bonding the semiconductor device main body and the interposer by a conductive film [solder] which has an adhesiveness and a conductivity in a pressed direction, the conductive film fixing the semiconductor device main body to the interposer and electrically connecting them; and an external connection terminal forming step of forming external connection terminals which are connected to the wiring pattern through holes formed in the base member and are arranged on a surface of the semiconductor device main body opposite to the surface on which the protruding electrodes are provided.

However, Yamaji does not appear to explicitly teach that the conductive film is an anisotropic conductive film.

Regardless, at column 3, line 54 to column 4, line 15, and column 5, lines 18-23, Pennisi teaches a bonding step of bonding an integrated circuit device main body 230 and a substrate 200 by an anisotropic conductive film 220 which has an adhesiveness and a conductivity in a pressed direction, the conductive film fixing the integrated circuit device main body to the substrate

and electrically connecting them. Furthermore, it would have been obvious to combine the process of Pennisi with the process of Yamaji because it would facilitate electrical connection.

Claim 90 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Ota (JP5343458) and Kihira (JP864725).

As cited supra, Ota teaches the following:

90. A method for fabricating a semiconductor device comprising: a mold preparing step of preparing a mold including a first mold 9a, and a second mold which is located so as to face the first mold, the second mold including a first half body 9b having a shape corresponding to a shape of a substrate, and a second half body 8b which is provided so as to surround the first half body and can be elevated with respect to the first half body, the first and second half bodies cooperating with each other so that a cavity to be filled with resin is defined; a resin sealing step of placing the substrate 5 on which a semiconductor element equipped with protruding electrodes 4 is formed in the mold and supplying resin 1 to positions in which the protruding electrodes are provided so as to form a resin layer which seals the protruding electrodes and the substrate.

However, Ota does not appear to explicitly teach a plurality of semiconductor elements, a protruding electrode

exposing step of exposing at least end portions of the protruding electrodes from the resin layer, and a separating step of cutting the substrate together with the resin layer so that the semiconductor elements are separated into each other.

Notwithstanding, as cited supra, Kihira teaches this process. In addition, it would have been obvious to combine the process of Kihira with the process of Ota because, as taught by Kihira, it would enable highly integrated packaging.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Customer Service whose telephone number is 703-306-3329.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is 703/3087724.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
22-Aug-02